TV Dazzler II Combo Board Bus Logic

to RAM
bDO7-bDO0
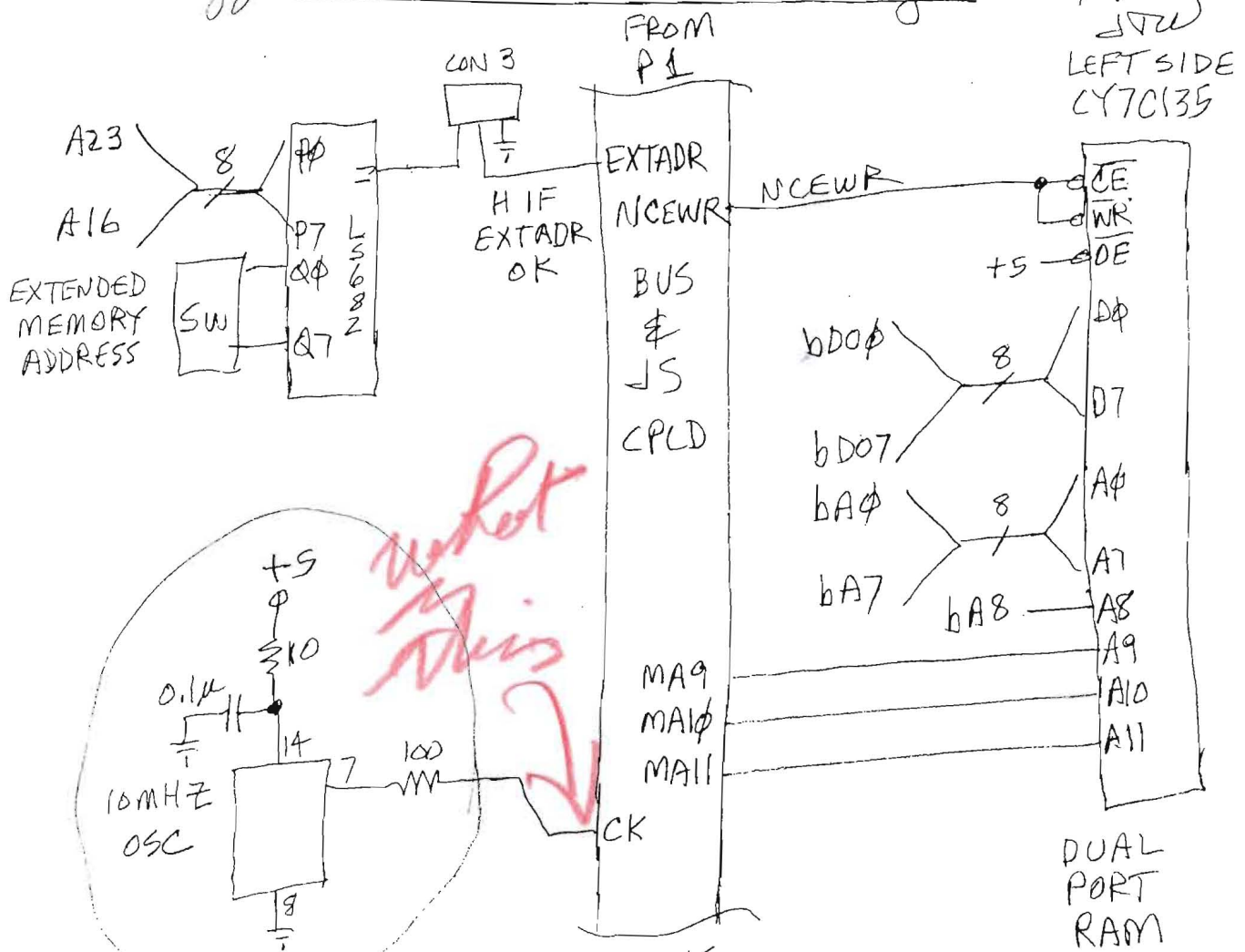
TO U1&U6

bA15
bA8
8
EXTENDED
PORT
BLOCK
SW 8

P0
L
S
P7 6
Q0 8
2
Q7

CoN 3

DO7
DO0
8
LS244
8
8

bDO7-0
BUS
&JS
CPLD

7
LS574
D Q
pt0F
b6-b0

H for TV Dazzler en → TVDEN

pt0FCK

b A7
b A1
7
DAZZLER
PORT
BASE
SW 7

P0
P1
L
S
P7 6
Q0 8
Q1 2
Q7

PWR
SOUT
SWO
PDBIN
SINP
5
LS244
5

bNPWR
bSOUT
bNSWO
bPDBIN
bSINP

FROM U1
pt0Eb7
" b6
TO U1
pt0Eb7

H for JSen → JSEN

bA7
bA3
5
JS
PORT
BASE
SW 5

P0
P1
L
S
P5
P6
P7
Q0 8
Q1 2
Q5
Q6
Q7

DI7
DI0
8
LS244
8
0LDI7-0

JSEN
NPTI8EN
LDI7-0
NIN

NPTI8EN

?

bA15
bA9
7
bA15
bA9

to RAM
bA7-bA0

A7
A0
8
LS244
8
bA7-bA0
8
3
A2
A1
A0
bA2
bA1
bA0

bA15-bA8
A15
A8
8
bA8 TO RAM

CONTINUED
ON P2

CBBL2

JTW)

LEFT SIDE
CY7C135

FROM
P1

CON 3

A23
8
A16

P0
P7
Q0
Q7

LS682

SW

EXTENDED
MEMORY
ADDRESS

H IF
EXTADR
OK

EXTADR
NCEWR

NCEWR

NCEWR

CE
WR
OE

+5

BUS
&
JS
CPLD

bDO0
8
bDO7

bA0
8
bA7   bA8

D0
D7

A0
A7
A8
A9
A10
A11

+5

+5

10

0.1μ

14
7   100

10MHZ
OSC

8

MA9
MAI0
MAII

CK

DUAL
PORT
RAM

use not this

TO JS
INTERFACE

We could use instead a
connection to the
CK8 (8.18 MHZ) oscillator
output of the Dazzler video
CPLD if it is not too long. (i.e. < 3 in)

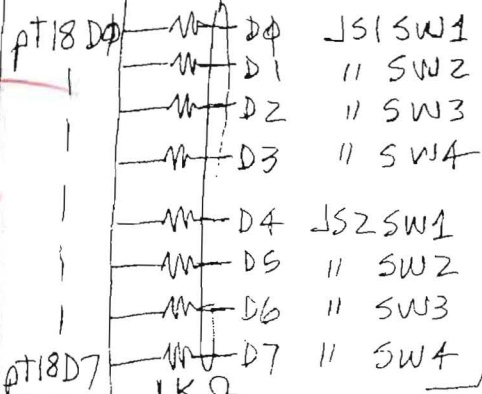# T.V Dazzler Combo Board Joystick Interface 3/8/16 3/4
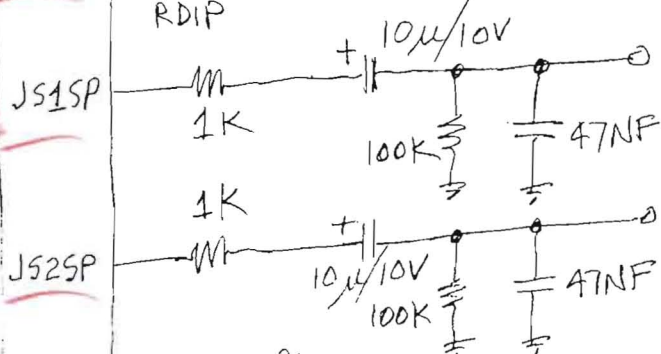JTW

RSIP → Provide on-board 10K pullups to +5
FROM PZ   port 18h IN   on connector side

pT18 D0	D0	JS1 SW1
	D1	" SW2
	D2	" SW3
	D3	" SW4
	D4	JS2 SW1
	D5	" SW2
	D6	" SW3
pT18 D7	D7	" SW4

1KΩ
RDIP

3/9 move to external buffer 74LS244
controlled by NPT18EN
omit 1K series resistor
See page 4 & 1

Speaker outputs use a PWM DAC in the CPLD
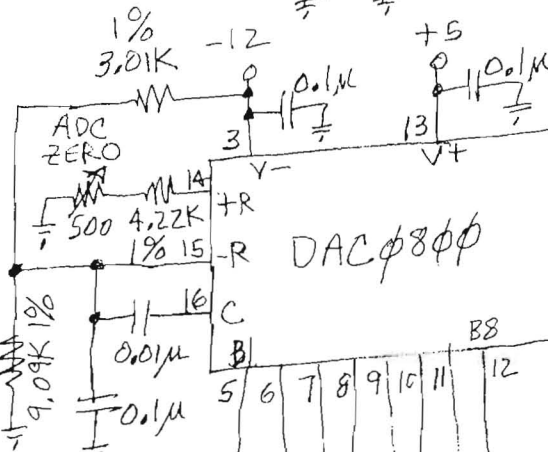JS1 speaker ±2.5V AC
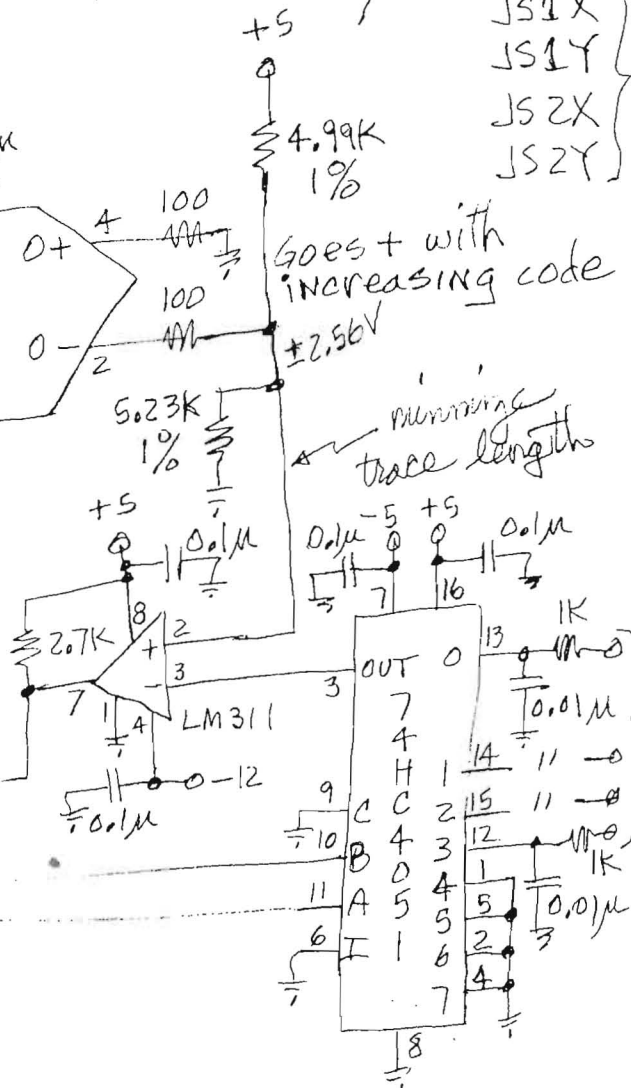100HZ → 4KHZ BW   ±2.5V IN DC
JS2 speaker ±2.5V

JS1SP 1K +10μ/10V o JS1 speaker
100K 47NF

1K
JS2SP +10μ/10V o JS2 speaker
100K 47NF

BUS & JS CPLD

Joystick CONNECTIONS
JS1 X
JS1 Y
JS2 X
JS2 Y

+5
4.99K
1%

1%
3.01K −12   +5
ADC ZERO 3 0.1μ 13 0.1μ
14 +R
500 4.22K
1% 15 −R   DAC0800
16 C
9.09K 1% 0.01μ
B
0.1μ
5 6 7 8 9 10 11 12 B8

4 0+ 100
0− 100
2
+2.56V
Goes + with increasing code

5.23K
1%
running trace length

+5 0.1μ
2.7K 8 2
+ LM311
7 3
4
−12
0.1μ

−5 +5
0.1μ 0.1μ
7 16 0.01μ

74HC4051

OUT 0 13 1K
3 7 0.01μ
9 1 14 "
C 2 15 "
B 4 3 12
A 0 5 1 1K
I 5 2 0.01μ
6 6 3
7 0.01μ
8

DAC1
DAC2
DAC3
DAC4
DAC5
DAC6
DAC7
DAC8
COMP
SELB
SELA

TV Dazzler II Bus Address Selector

3/6/16 JTW

D0
D7

LS244

D0
D7
A0
A8
A9
A10
A11
WE
CE

CY7C135

LS244

A0
|
A8

9

S100 bus

A9
|
A15

SUBTRACTOR

L if dif is < 0

LS283

A9, A10, A11

A12-15

Cout
A
Σ
B
CIN

7

3

4

base mem addr port

A9
|
A15

LS240
1's comp

7

H

+1 for 2's comp

L to prevent writing

WE

Subtract, base starting address

H if extended address or page not OK

$Cout = L$ if base # > S100 address

$A12 \cdots \dagger A15 = H$ if $(S100 - base\#) \geqslant 2^{12}$

Use this One
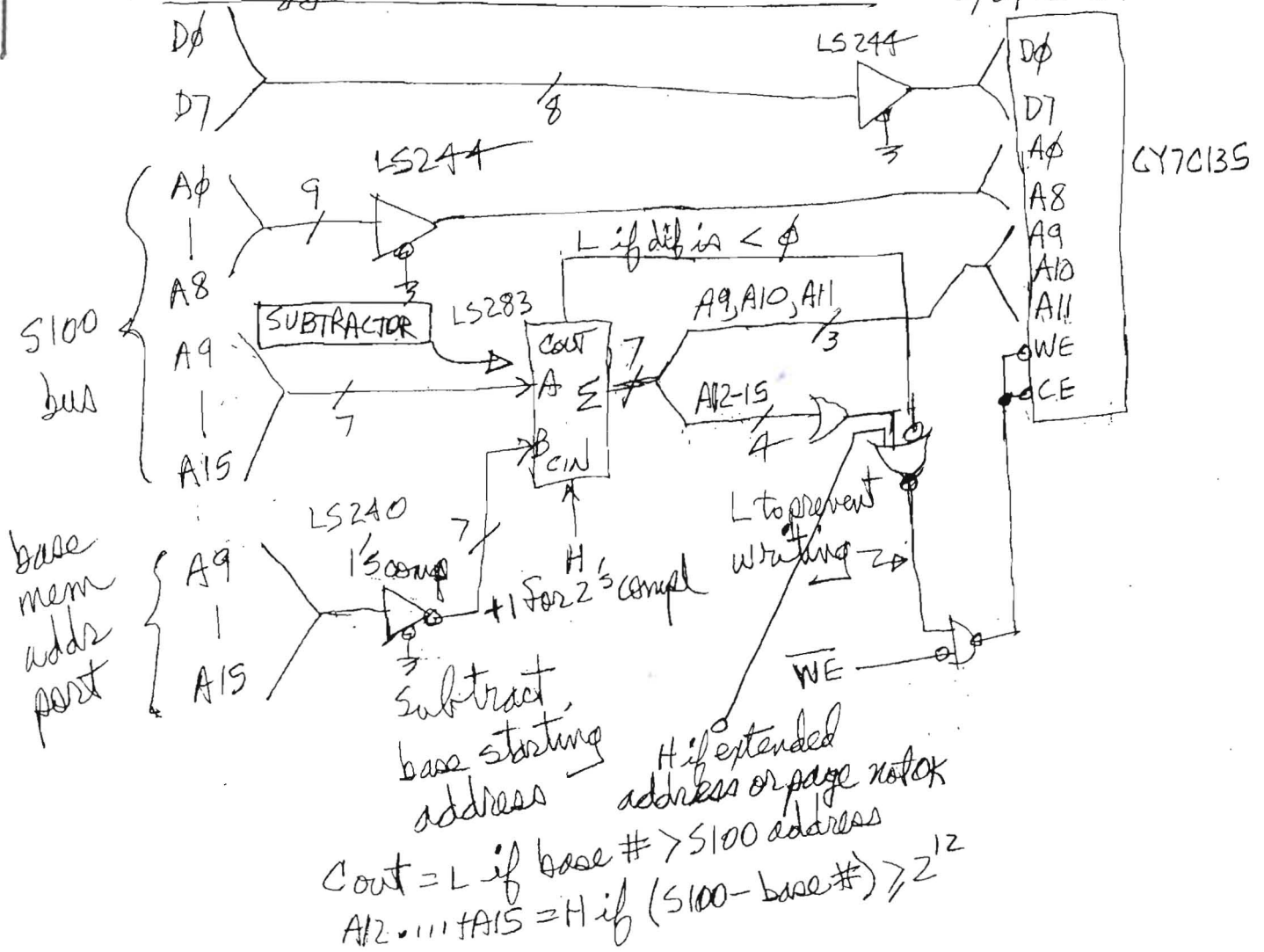
Is this within a CPLD or do we need to do it in hardware